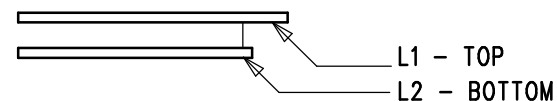


REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	PRODUCTION	JON M.	09-05-12

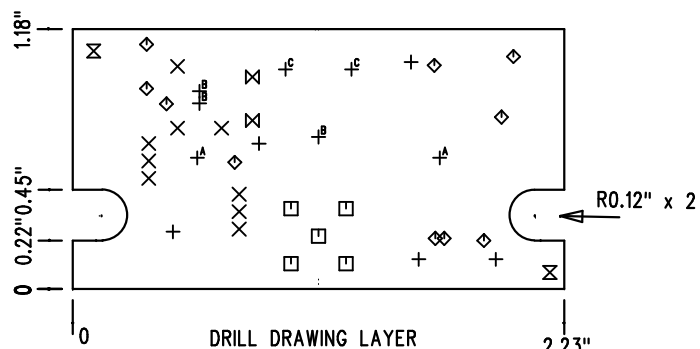
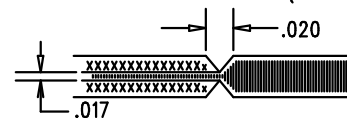
LAYER STRUCTURE



NOTES: UNLESS OTHERWISE SPECIFIED


- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.
-FINISHED THICKNESS TO BE 0.062" +/- .005"
-TOTAL OF 2 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS

-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.
-GOLD IMMERSION BOTH SIDES.
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



DRILL DRAWING LAYER
LINEAR TECHNOLOGY DATE: 09-05-12
DC1979A-2 LTC6090CS8E
HIGH-VOLTAGE CMOS AMPLIFIER

SIZE	QTY	SYM	PLATED	TOL
0.066	5	+	YES	+/-0.003
0.035	9	X	YES	+/-0.003
0.055	5	□	YES	+/-0.003
0.01	10	◇	YES	+/-0.003
0.07	2	⊗	NO	+/-0.003
0.03	2	⊗	YES	+/-0.003
0.125	2	+ ^A	NO	+/-0.003
0.04	3	+ ^B	YES	+/-0.003
0.075	2	+ ^C	YES	+/-0.003

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION		APPROVALS		 LINEAR TECHNOLOGY 1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL - FOR CUSTOMER USE ONLY	
		PCB DES.	AK		
		APP ENG.	JON M.	TITLE: FABRICATION DRAWING	
				HIGH-VOLTAGE CMOS AMPLIFIER	
		SIZE	IC NO.	LTC6090CS8E	REV
		N/A		DEMO CIRCUIT 1979A	2
SCALE = NONE		FILENAME: DC1979A-2.PCB			SHT 1 OF 1